Sierra Components, Inc.
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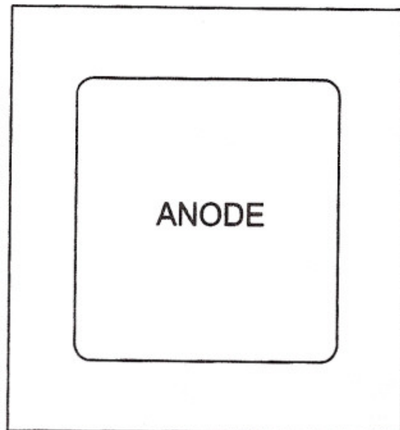
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	14 X 14 MILS
Die Thickness	7.5 MILS
Anode Bonding Pad Area	9.5 X 9.5 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 14,000Å

GEOMETRY



GROSS DIE PER 4 INCH WAFER
61,141

PRINCIPAL DEVICE TYPES
CMPZ5221B
THRU
CMPZ5234B

APPROVED BY:MG	DIE SIZE :14 x 14 Mils	DATE: 2/1/10
MFG:Central Semi	THICKNESS:	P/N:CMPZ5231B

DG 10.1.2
Rev B, 7/19/02